II. AMENDMENTS TO THE CLAIMS

The following listing of claims replaces the previous listing of claims.

1. (Currently amended) A transceiver for receiving and transmitting data over a network, comprising:

a transmitter for receiving a network data signal representative of a signal capable of being transmitted over a network and a control signal for impairing characteristics of the network data signal, and for continuously generating an output signal corresponding to the data signal and the control signal during a predetermined time window;

a receiver for continuously receiving the output signal from the transmitter, and for reconstructing the network data signal within the predetermined time window; and

a built-in-self-test (BIST) device for generating the network data signal and the control signal, and for providing a clock signal with a varied offset for jitter testing of the network data signal, wherein the BIST device detects erroneous performance by the transceiver based on the reconstructed network data signal.

2. (Original) The transceiver of claim 1, wherein the control signal includes signals for impairing a phase and an amplitude of the network data signal.

3. (Original) The transceiver of claim 1, wherein the BIST device includes a jitter control system .

4. (Original) The transceiver of claim 3, wherein the jitter control system varies an offset of a clock signal.

5. (Original) The transceiver of claim 3, wherein the jitter control system comprises:

a multiplexor for outputting the clock signal;

at least one delay timer for delaying an input clock signal;

a shift register for controlling the multiplexor; and

a controller for controlling the multiplexor and updating the shift register.

6. (Original) The transceiver of claim 1, wherein the BIST device further comprises a pulse width counter for varying a pulse width of the network data signal.

7. (Original) The transceiver of claim 6, wherein the pulse width counter tests a clock recovery capability of the receiver.

8. (Original) A transceiver for receiving and transmitting data over a network, comprising:

a transmitter for receiving a network data signal representative of a signal capable of being transmitted over a network and a control signal for impairing characteristics of the network data signal, and for continuously generating an output signal corresponding to the data signal and the control signal during a predetermined time window;

a receiver for continuously receiving the output signal from the transmitter, and for reconstructing the network data signal within the predetermined time window; and

a built-in-self-test (BIST) device for generating the network data signal and the control signal, and for varying a pulse width of the network data signal, wherein the BIST device comprises means for detecting erroneous performance by the transceiver based on the reconstructed network data signal.

9. (Original) The transceiver of claim 8, wherein the control signal includes signals for impairing a phase and an amplitude of the network data signal.

10. (Original) The transceiver of claim 8, wherein the BIST device comprises means for programming the network data signals.

11. (Original) The transceiver of claim 8, wherein the transmitter and the receiver are provided on a single integrated circuit, the transceiver further comprising a transfer gate for selectively coupling the output signal from the transmitter to the receiver within the integrated circuit.

12. (Original) The transceiver of claim 8, wherein the network data signal includes an embedded clock signal, and wherein the BIST device comprises means for locking onto the embedded clock signal.

13. (Original) The transceiver of claim 12, wherein the means for detecting erroneous performance by the transceiver comprises a counter device for counting edge transitions of the

clock signal for establishing a time window for reconstructing the network data signal data recovered from the output signal.

14. (Original) The transceiver of claim 13, wherein the means for detecting erroneous performance by the transceiver further comprises a counter device for counting edge transitions of the network data signal within the established time window.

15. (Original) A method for testing performance of a transceiver for receiving and transmitting data over a network, comprising the steps of:

generating a network data signal representative of signals capable of being transmitted over a network, and generating a control signal for impairing characteristics of the network data signal;

varying a pulse width of the network data signal;

varying an offset of a clock signal embedded within the network data signal;

a transmitter component of the transceiver device receiving the network data signal and the control signal and generating an output signal corresponding to the network data signal and having an impaired characteristic according to the control signal, the output signal being generated continuously during a predetermined time window;

a receiver component of the transceiver device continuously receiving the output signal from the transmitter component and reconstructing the network data signal within the predetermined time window; and

detecting erroneous performance by the transceiver based on the reconstructed data signal.

16. (Original) The method of claim 15, wherein the step of reconstructing the network data signal comprises counting edge transitions of the embedded clock signal to establish the predetermined time window.

17. (Original) The method of claim 15, wherein the step of reconstructing the network data signal comprises counting edge transitions of the network data signal within the predetermined time window.

18. (Original) A program product stored on a recordable medium for testing a transceiver device, which when executed, comprises:

program code for generating a network data signal representative of data capable of being transmitted over a network by a transceiver device and for generating a control signal for impairing characteristics of the network data signal;

program code for varying a pulse width of the network data signal;

program code for varying an offset of a clock signal embedded within the network data signal;

program code for enabling a transmitter component of the transceiver device to receive said network data signal and the control signal, and for generating an output signal corresponding to the network data signal having an impaired characteristic according to the control signal, wherein the output signal is generated continuously during a predetermined time window;

program code for enabling a receiver component of the transceiver device to continuously receive the output signal from the transmitter component and for reconstructing the network data

signal within the predetermined time window; and

program code for detecting erroneous performance by the transceiver device based on the reconstructed network data signal.

19. (Original) The program product of claim 18, wherein the program code for reconstructing the network data signal comprises program code for counting edge transitions of the embedded clock signal to establish the predetermined time window.

20. (Original) The program product of claim 18, the program code for reconstructing the network data signal comprises program code for counting edge transitions of the network data signal within the predetermined time window.